3.5 A 5.4mW 2-Channel Time-Interleaved Multi-bit ΔΣ Modulator with 80dB SNR and 85dB DR for ADSL

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A 2-channel time-interleaved (TI) 2nd-order ΔΣ modulator is presented. This achieves a FOM of 0.48pJ/conversion-level where FOM=power/[$2^{(SNDR-1.76)/6.02}\times 2\times$BW]. It targets broadband applications including ADSL. The power consumption of the modulator is reduced by time-interleaving which enables the internal circuits to operate at a slower clock rate and the simplified architecture; it can be implemented with only 2 opamps. Furthermore, this structure is robust to channel mismatches and uses a simple clocking scheme. The circuit is implemented in a 0.18μm CMOS process with MIM capacitors.

Figure 3.5.1 shows the conventional 2nd-order ΔΣM where only one output, $y(n)$, is generated per each time slot n. For the equivalent 2-channel TI modulator, outputs $y(2n)$ and $y(2n+1)$ are simultaneously generated [1]. Figure 3.5.2 shows the proposed 2-channel TI structure where $y_1(n)$ and $y_2(n)$ each corresponds to $y(2n)$ and $y(2n+1)$. In this scheme, the second output $y_2(n)$ is generated by directly quantizing the 1st-integrator output $2p_{11}(n)$. This eliminates the extra active block and reduces the number of levels for Q_2 and DAC_2 as compared to [2]. In addition, the proposed structure does not require a complex clocking scheme as in [1] where the actual implementation of a 2-channel 2nd-order ΔΣM needs 4 opamps. Noting that $p_{22}(n) = p_{21}(n) + 2p_{11}(n) - 2y_1(n)$, the input of Q_2 is

$$p^*_{22}(n)=2p_{11} = p_{22}(n)-p_{21}(n)+2y_1(n) \quad (1)$$

where $p_{21}(n)$ and $p_{22}(n)$ each corresponds to $p_2(2n)$ and $p_2(2n+1)$ of Fig. 3.5.1. The quantization of $p^*_{22}(n)$ leads to $y^*_2(n) = y_2(n) + y_1(n)$, since $Q[p_{22}(n)] = y_2(n)$ and $Q[p_{21}(n)] = y_1(n)$. Therefore, $y_2(n)$ can be simply obtained by subtracting $y_1(n)$ from the output of Q_2 in the digital domain. Furthermore, the input sampling block is simplified by removing an input branch (path1 in Fig. 3.5.2). However, the performance of the modulator is not affected even without the input filter $(1+z^{-1})$ as long as the OSR is greater than the number of channels. The output swing of the 2nd-integrator is further reduced by removing the input feed-forward branch (path2 of Fig. 3.5.2), which decreases the number of levels for Q_1 and DAC_1.

The transfer function of the proposed 2-channel TI modulator is obtained by combining the channel outputs $y_1(n)$ and $y_2(n)$, in the z-domain. That is

$$Y_1(z^2) + z^{-1}Y_2(z^2) = z^{-3}[X_1(z^2)] + (1-z^{-1})^2[\varepsilon_1(z^2) + z^{-1}\varepsilon_2(z^2) + z^{-1}\varepsilon_1(z^2)] \quad (2)$$

where ε_1 and ε_2 are the quantization errors of Q_1 and Q_2, respectively. Although Equation (2) shows a 2nd-order noise-shaping feature, an extra error term $z^{-1}\,\varepsilon_1(z^2)$ is present. Therefore, the shaped-quantization-noise power is doubled as compared to the original structure in [2]. This leads to an SNR degradation of 3dB which is minor, considering the simplified hardware. As a result, the SNR improvement is 12dB with respect to the conventional modulator shown in Fig. 3.5.1, assuming that both modulators are operating at the same internal clock rate.

Channel mismatch in TI ΔΣMs can increase the in-band noise level and cause tones that fall in the signal band [1]. The main error source is the mismatch of the DACs performing the global feedback operation. However, the proposed structure is robust to channel mismatches due to the single global feedback path. Moreover, the local DAC in the 2nd-integrator feedback is not critical. Since, the possible gain error of DAC_1 and DAC_2 which cause feedback path mismatches are all 1st-order shaped by the loop filter operation. Even using two quantizers is not problematic, since the offset and input-common-mode variation of Q_1 and Q_2 are all 2nd-order shaped. However, the effect of the 1st-integrator phase error due to the finite dc gain of the opamp is much severe than the conventional 2nd-order ΔΣM, since the phase error of the first integrator generates a non-shaped error term in the noise transfer function. This requires an opamp with a higher dc gain. The integrator gain error owing to capacitor mismatches and improper settling of the output is less critical compared to the integrator phase error. Since, the gain error of the first and second integrator are 1st-order and 2nd-order shaped, respectively.

The signal bandwidth of the proposed ΔΣM is 1.1MHz with OSR=60. This leads to an effective sampling rate $f_{s,eff}$=132MHz whereas the internal circuits operate at the reduced clock rate of f_s=66MHz. Furthermore, to achieve a 13b resolution, the opamp dc gain for the first and second integrator should be at least 70dB and 50dB, respectively. The sampling capacitors are set to 1.6pF and 0.8pF for the first and second integrator, considering the kT/C noise limit. The output swing of the first and second integrator is $\pm V_{REF}$ and $\pm 0.6V_{REF}$, respectively.

Figure 3.5.3 shows the SC implementation of the modulator. Both integrators share the sampling capacitors with the DAC. This alleviates the GBW requirement of the opamps by improving the feedback factor of the integrator. The input common-mode voltage of the integrators is lowered to 0.4V to ensure proper charge transfer for the NMOS switches connected to the input node of the opamps [3]. This enables using small sized NMOS switches which reduces the clock feed-through mismatch. In addition, bottom-plate sampling technique is used to eliminate the channel charge injection of the remaining CMOS switches. A 2-stage opamp is used for the first integrator to meet the high dc gain and output swing requirements. The relaxed requirements for the second integrator enable the use of a single-stage opamp. Individual level averaging (ILA) scheme is used in the feedback of the first integrator to shape the tones caused by the element mismatches.

Figure 3.5.4 shows the measured 65536-point FFT output spectrum for a -6dBFS, 201.45kHz sine-wave input. The alias tone at $f_{s,eff}/2 - f_{in}$ does not overload the modulator. Figure 3.5.5 shows the SNR and the SNDR plots versus input amplitude. The peak SNR and peak SNDR is 80dB and 76dB, respectively with DR of 85dB. The total power consumption excluding the reference buffer and the digital output drivers is 5.4mW where half of the analog power is consumed in the first integrator. The modulator performance is summarized in Fig. 3.5.6. Figure 3.5.7 shows the chip micrograph which has an active area of 1.1mm^2.

Acknowledgements:
The authors wish to thank Dr. J. Koh for helpful comments, and C. Kim for the chip testing. Dr. J. Koh and C. Kim are with the Texas Instruments, Dallas, TX.

References:
[1] R. K. Poorfard, L. B. Lim, and D. A. Johns, "Time-Interleaved Oversampling A/D Converters: Theory and Practice," *IEEE Trans. Circuits Syst. II*, vol. 44, no. 8, pp. 634-645, Aug., 1997.
[2] K. Lee and F. Maloberti, "Time-Interleaved Sigma-Delta Modulator Using Output Prediction Scheme," *IEEE Trans. Circuits Syst. II*, vol. 51, no. 10, pp. 537-541, Oct., 2004.
[3] S. Rabii and B. A. Wooley, "A 1.8-V Digital Audio Sigma-Delta Modulator in 0.8-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 32, no. 6, pp. 783-796, June, 1997.

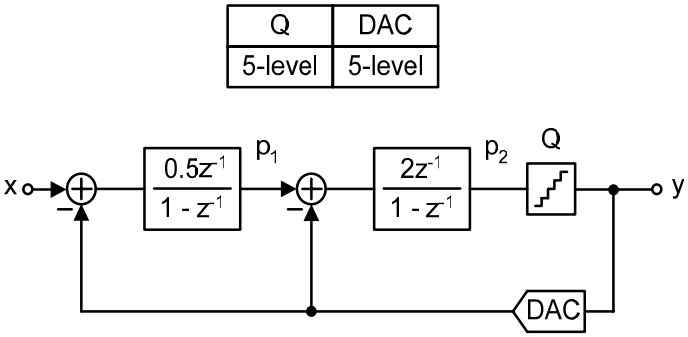

Figure 3.5.1: Conventional 2nd-order ΔΣM.

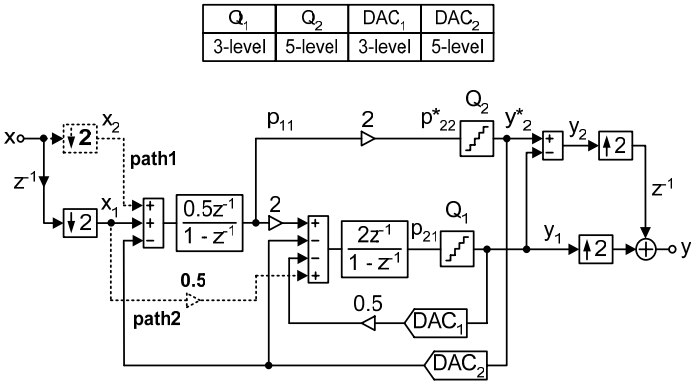

Figure 3.5.2: Proposed 2-channel ΔΣM.

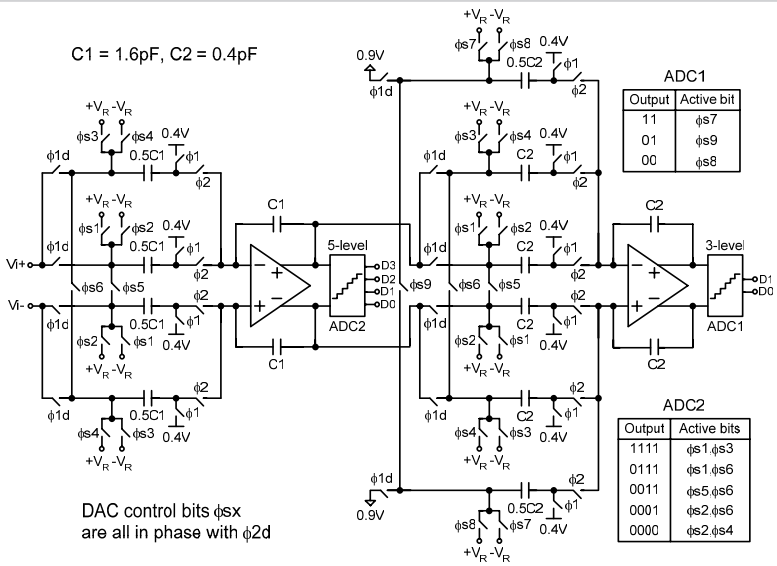

Figure 3.5.3: SC implementation.

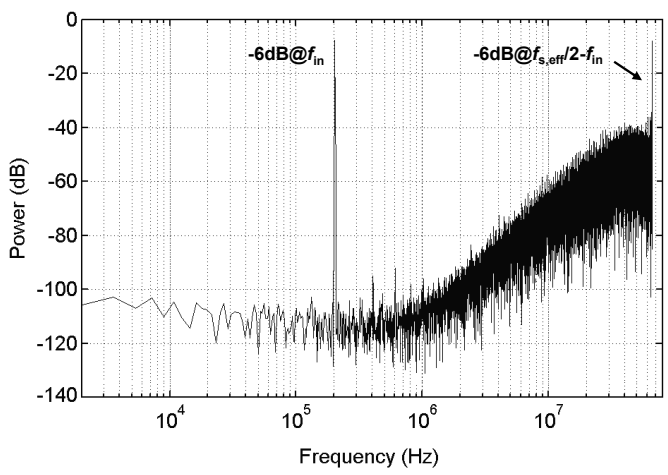

Figure 3.5.4: Measured output spectrum with -6dBFS input.

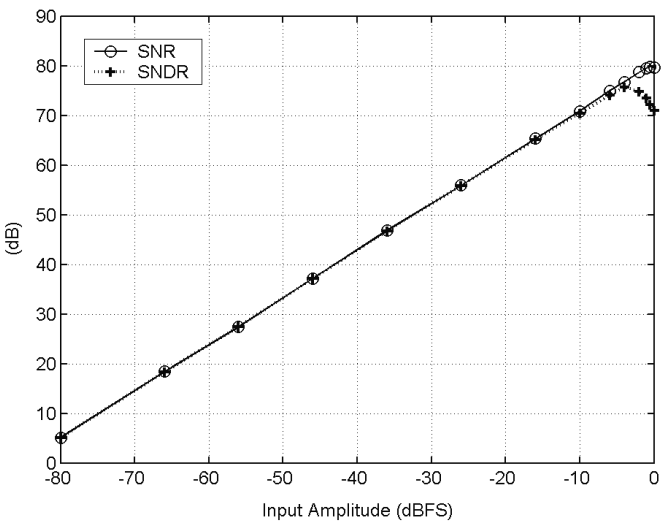

Figure 3.5.5: SNR and SNDR versus input amplitude.

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Supply voltage	1.8V
Effective sampling freq.	132MHz
Signal bandwidth	1.1MHz
OSR	60
Reference voltage	0.8V
Input range (differential)	$1.6V_{pp}$
Peak SNR @ 201.45kHz	80dB
Peak SNDR @ 201.45kHz	76dB
DR	85dB
Power consumption	4.2mW (analog) 1.2mW (digital)
Core area	$1.1mm^2$
Technology	0.18μm CMOS

Figure 3.5.6: Modulator performance summary.

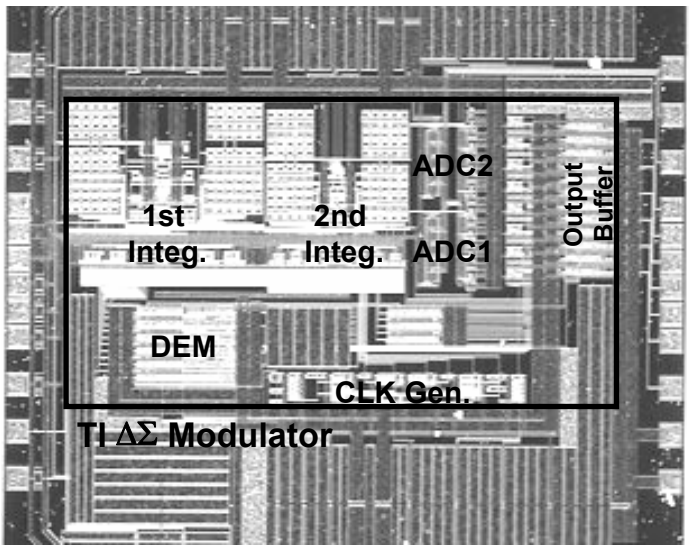

Figure 3.5.7: Chip micrograph.